# SN65MLVD20xB Multipoint-LVDS Line Drivers and Receivers With IEC ESD Protection

## 1 Features

- Compatible with the M-LVDS Standard TIA/EIA-899 for Multipoint Data Interchange
- Low-Voltage Differential 30-Ω to 55-Ω Line Drivers and Receivers for Signaling Rates(1) Up to 100 Mbps, Clock Frequencies up to 50 MHz
  - Type-1 Receiver Incorporates 25 mV of Hysteresis (200B and 202B)
  - Type-2 Receiver Provides an Offset Threshold to Detect Open-Circuit and Idle-Bus Conditions (204B and 205B)
- Bus I/O Protection
  - >±8-kV HBM
  - >±8-kV IEC 61000-4-2 Contact Discharge
- Controlled Driver Output Voltage Transition Times for Improved Signal Quality
- -1-V to 3.4-V Common-Mode Voltage Range Allows Data Transfer With 2 V of Ground Noise
- Bus Pins High Impedance When Disabled or $V_{CC}$ ≤ 1.5 V
- 200-Mbps Devices Available (SN65MLVD201, 203, 206, 207)
- Improved Alternatives to SN65MLVD200A, 202A, 204A and 205A

(1) The signaling rate of a line is the number of voltage transitions that are made per second expressed in the bps of the unit (bits per second).

## 2 Applications

- Low-Power, High-Speed, and Short-Reach Alternative to TIA/EIA-485
- Backplane or Cabled Multipoint Data and Clock Transmission
- Cellular Base Stations
- Central Office Switches
- Network Switches and Routers

## 3 Description

The SN65MLVD200B, SN65MLVD202B, SN65MLVD204B and SN65MLVD205B devices are multipoint-low-voltage differential (M-LVDS) line drivers and receivers which are optimized to operate at signaling rates up to 100 Mbps. This device family has robust 3.3-V drivers and receivers in the standard SOIC footprint for demanding industrial applications. The bus pins are robust to ESD events, with high levels of protection to human-body model and IEC contact discharge specifications.

These devices each combine a differential driver and a differential receiver, which operate from a single 3.3-V supply. The transceivers are optimized to operate at signaling rates up to 100 Mbps.

The SN65MLVD20xB have enhancements over similar devices. Improved features include a controlled slew rate on the driver output to help minimize reflections from unterminated stubs resulting in better signal integrity. The same footprint definition was maintained making for an easy drop-in replacement for a system performance upgrade. The devices are characterized for operation from –40°C to 85°C.

**Device Information(1)**

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| SN65MLVD200B(2) | SOIC (8) | 4.90 mm × 3.91 mm |
| SN65MLVD204B | | |
| SN65MLVD202B(2) | SOIC (14) | 8.65 mm × 3.91 mm |
| SN65MLVD205B(2) | | |

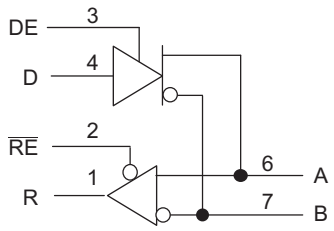
(1) For all available packages, see the orderable addendum at the end of the datasheet.

(2) Product Preview

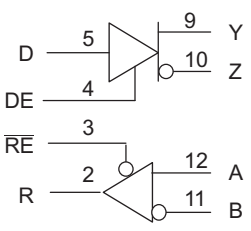
PRODUCT PREVIEW

## 4 Simplified Schematic

**SN65MLVD200B, SN65MLVD204B**




**SN65MLVD202B, SN65MLVD205B**

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# 5 Device and Documentation Support

## 5.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 1. Related Links**

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---|---|---|---|---|---|
| SN65MLVD200B | Click here | Click here | Click here | Click here | Click here |
| SN65MLVD202B | Click here | Click here | Click here | Click here | Click here |
| SN65MLVD204B | Click here | Click here | Click here | Click here | Click here |
| SN65MLVD205B | Click here | Click here | Click here | Click here | Click here |

## 5.2 Trademarks

All trademarks are the property of their respective owners.

## 5.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 5.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 6 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PRODUCT PREVIEW


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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN65MLVD204BD | PREVIEW | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | MF204B | |
| SN65MLVD204BDR | PREVIEW | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | MF204B | |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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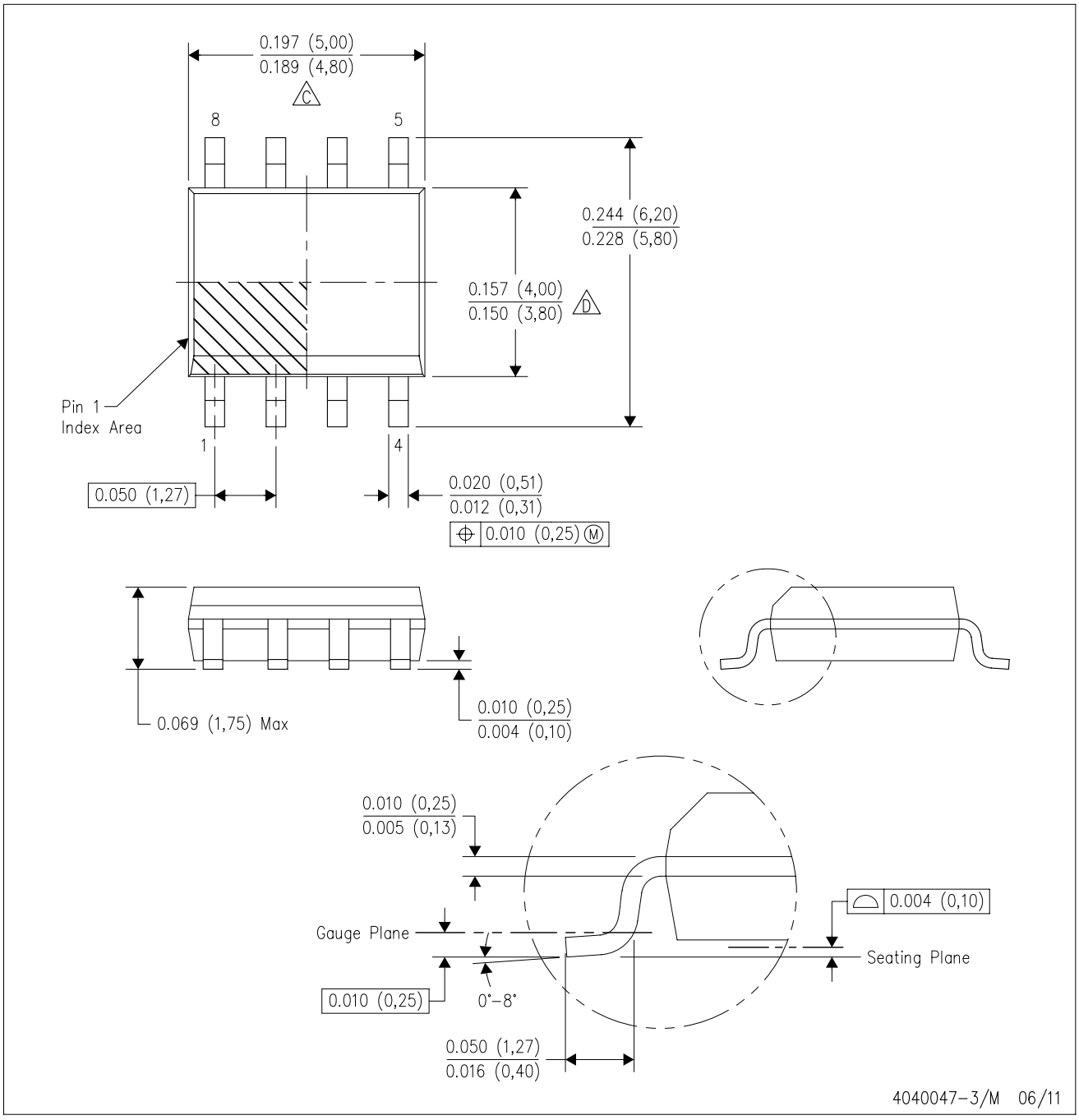
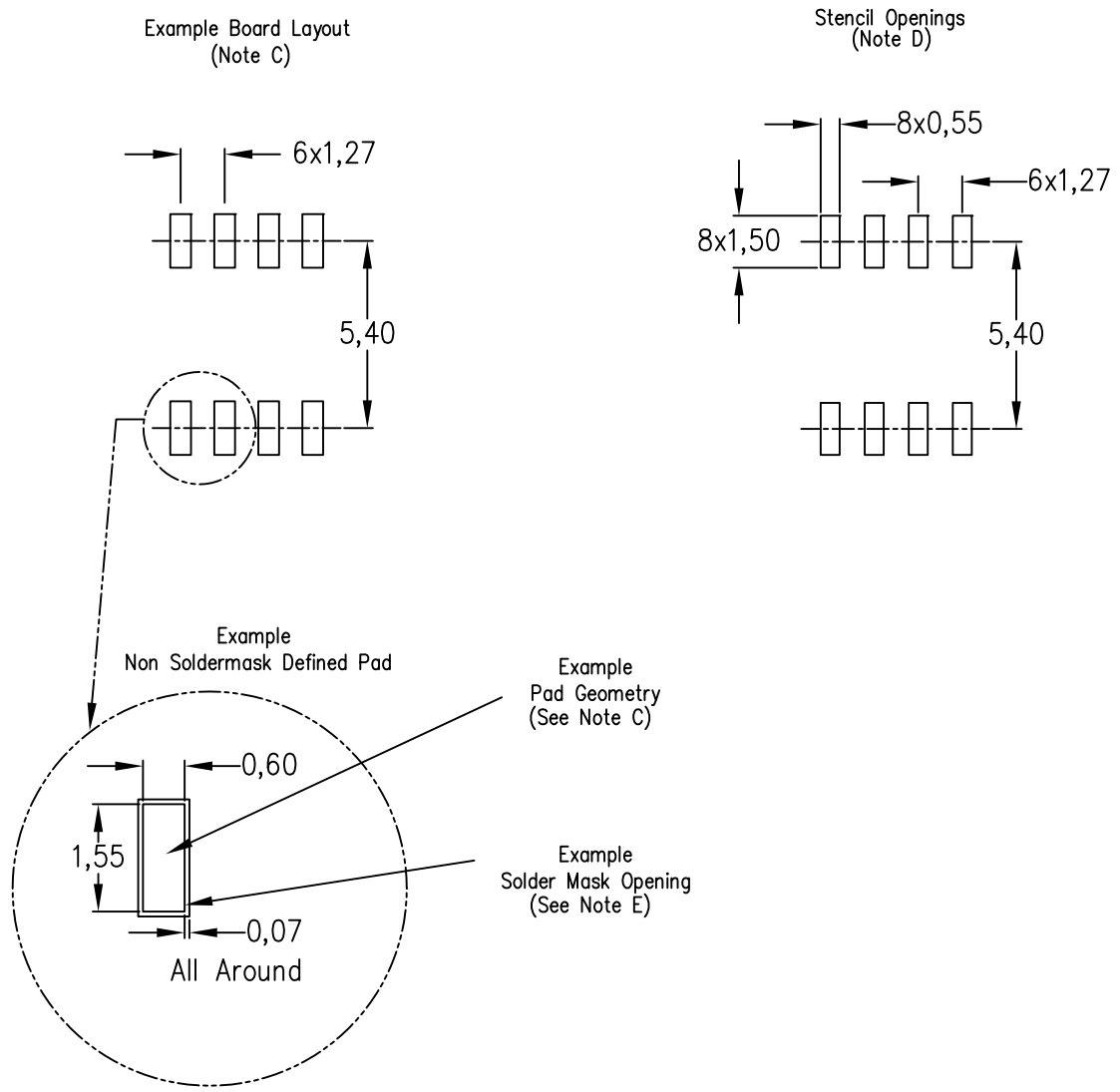
D (R–PDSO–G8) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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